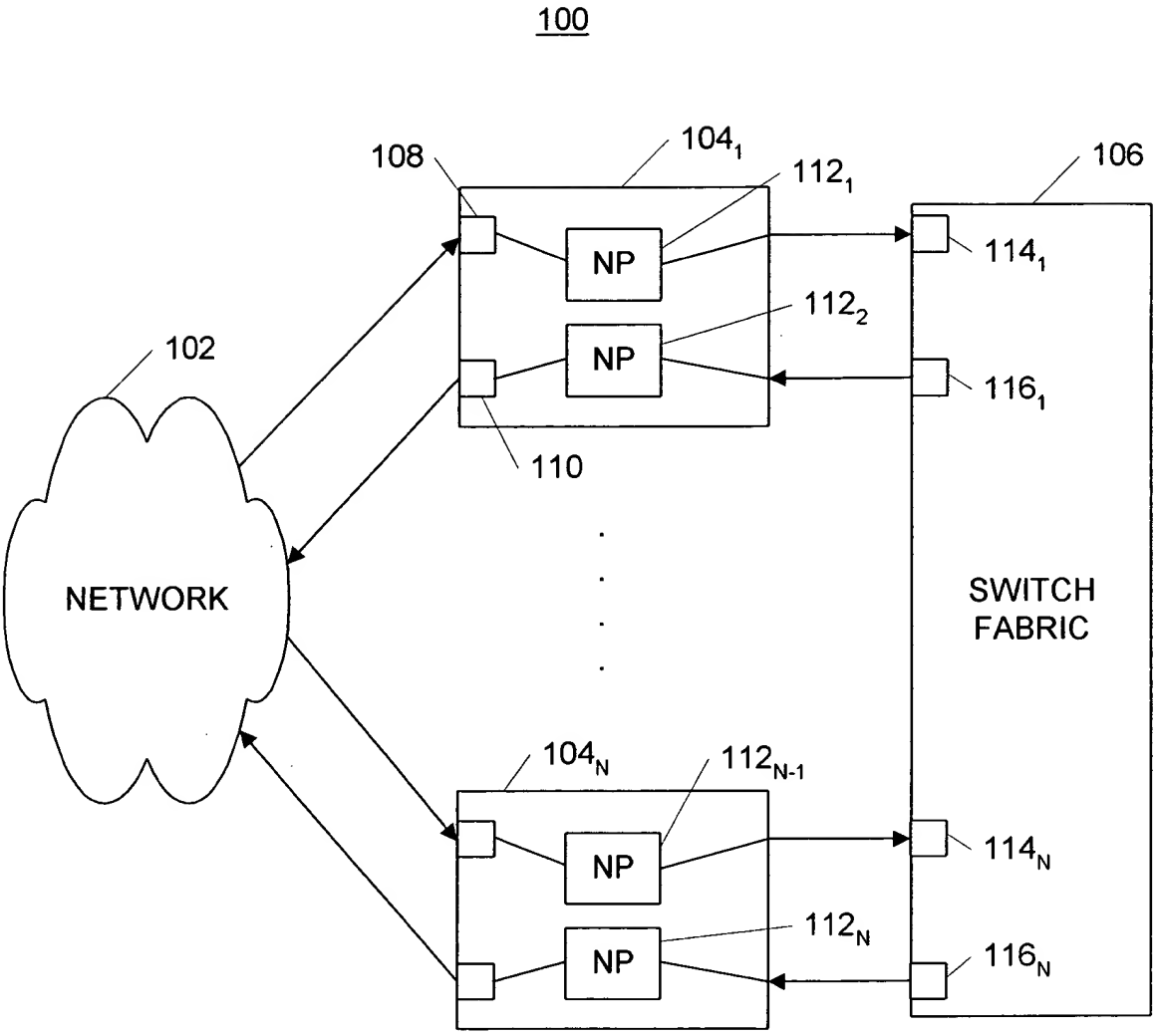
100
108
104_1
112_1
106
NP
114_1
112_2
NP
102
116_1
110
NETWORK
SWITCH
FABRIC
104_N
112_{N-1}
NP
114_N
112_N
NP
116_N

FIG. 1

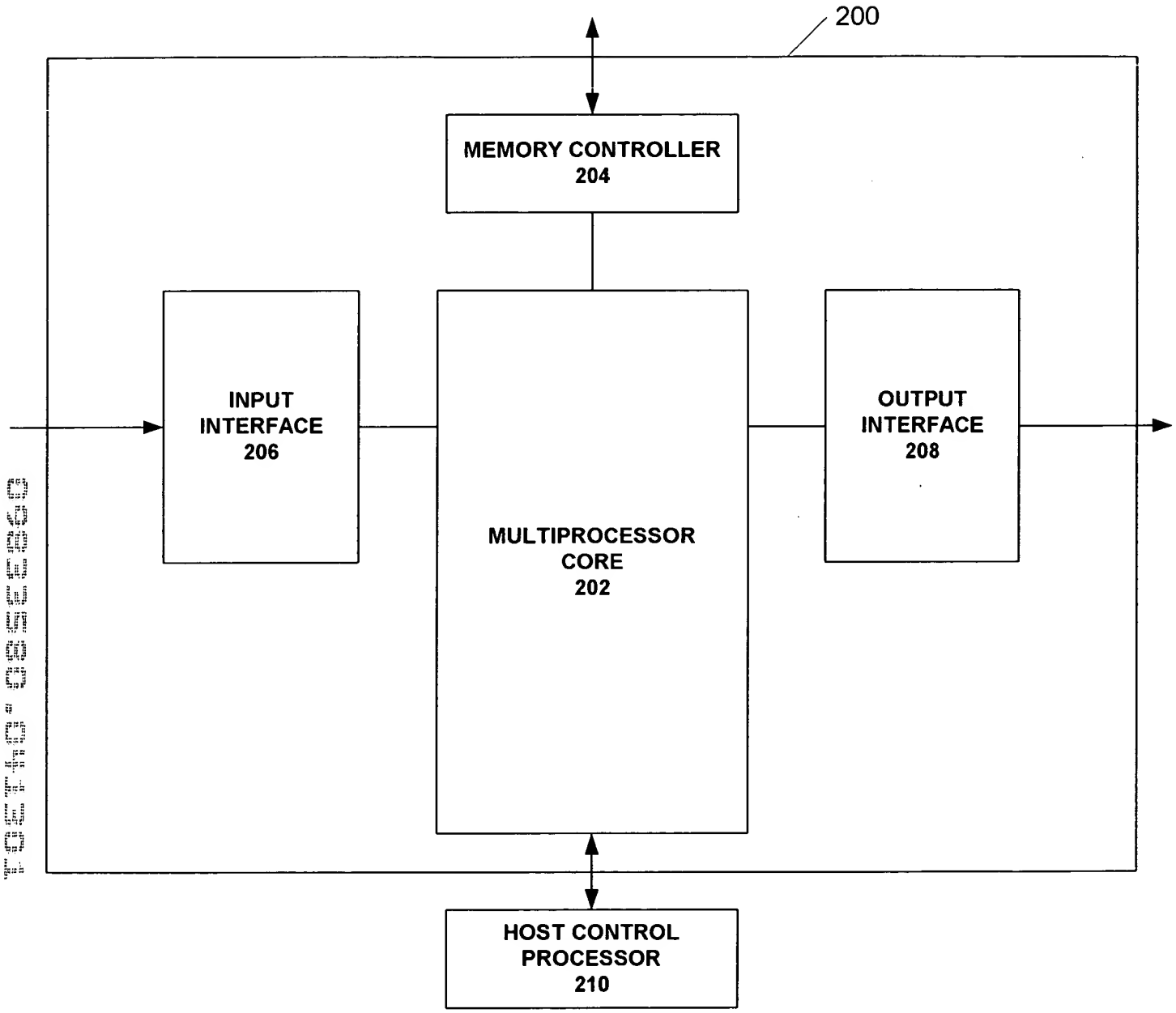
200
MEMORY CONTROLLER
204
INPUT
INTERFACE
206
MULTIPROCESSOR
CORE
202
OUTPUT
INTERFACE
208
HOST CONTROL
PROCESSOR
210

FIG. 2

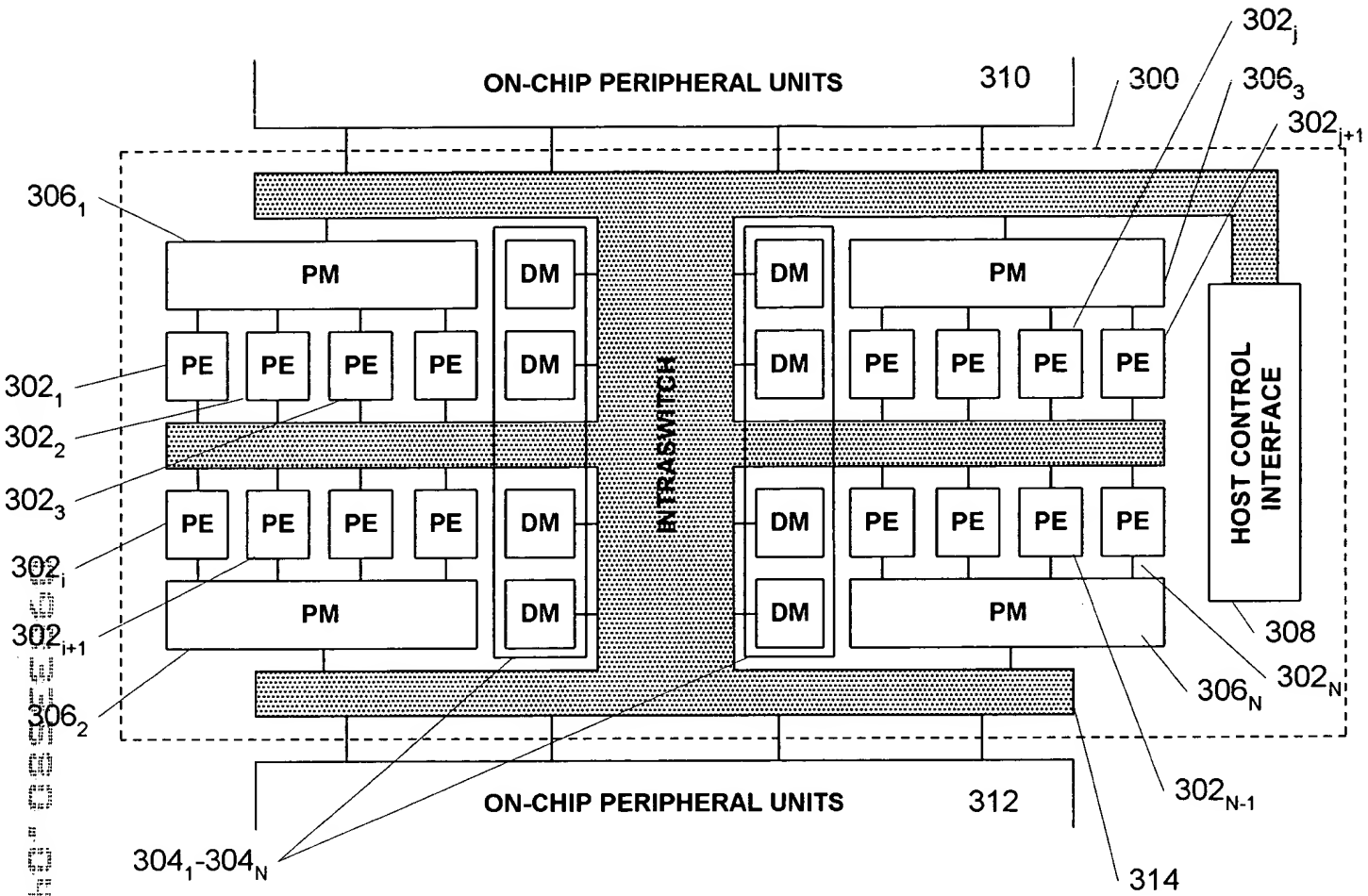
ON-CHIP PERIPHERAL UNITS
310
300
302_j
306_3
302_{i+1}
306_1
PM
DM
PE
302_1
302_2
302_3
302_i
302_{i+1}
306_2
INTRA-SWITCH
HOST CONTROL INTERFACE
308
306_N
302_N
302_{N-1}
ON-CHIP PERIPHERAL UNITS
312
304_1-304_N
314
PM: PROGRAM MEMORY
DM: DATA MEMORY
PE: PROCESSING ELEMENT

FIG. 3

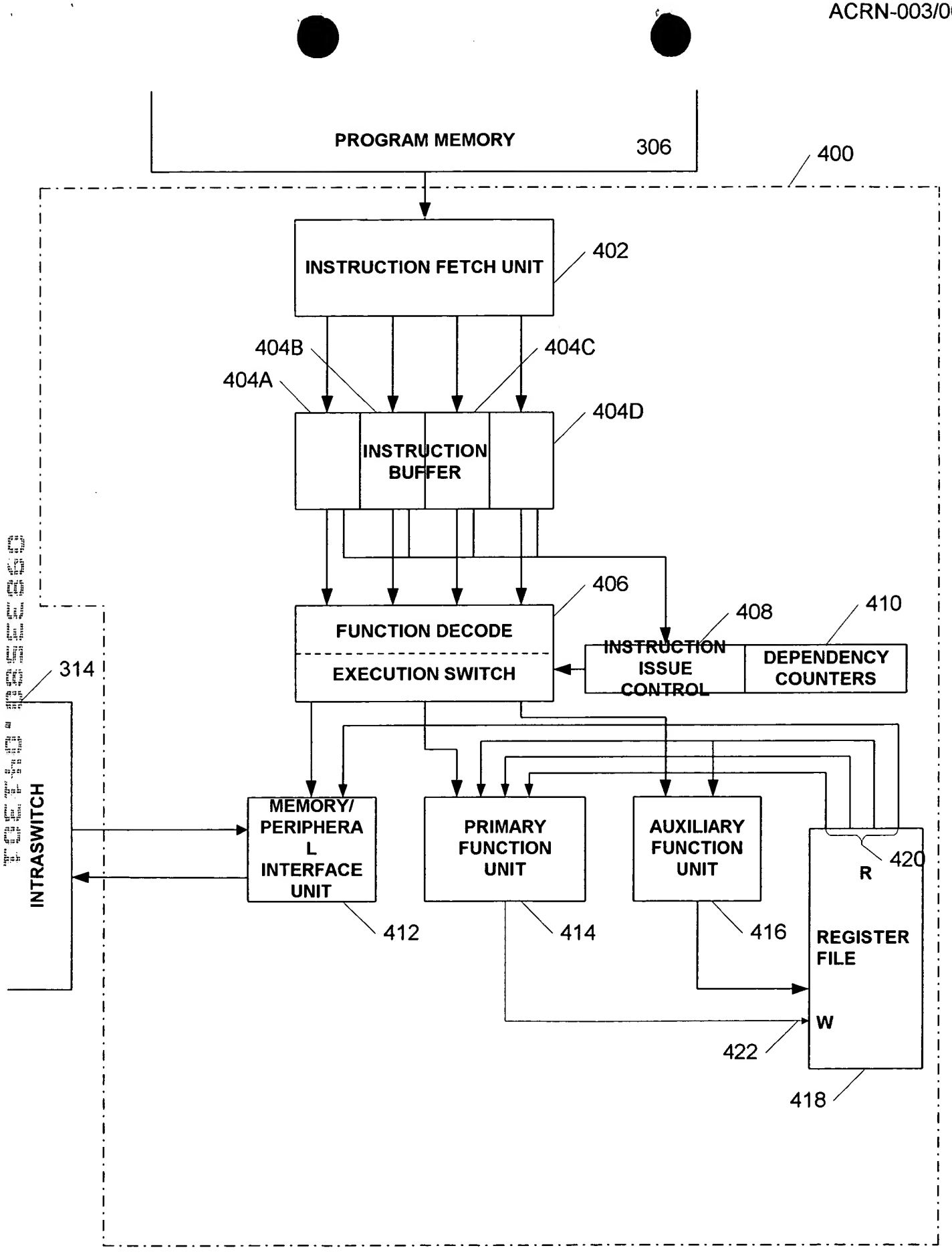
PROGRAM MEMORY
306
400
INSTRUCTION FETCH UNIT
402
404B
404C
404A
404D
INSTRUCTION BUFFER
406
FUNCTION DECODE
EXECUTION SWITCH
408
INSTRUCTION ISSUE CONTROL
410
DEPENDENCY COUNTERS
314
INTRASWITCH
MEMORY/ PERIPHERAL INTERFACE UNIT
412
PRIMARY FUNCTION UNIT
414
AUXILIARY FUNCTION UNIT
416
R
420
REGISTER FILE
W
422
418

FIG. 4

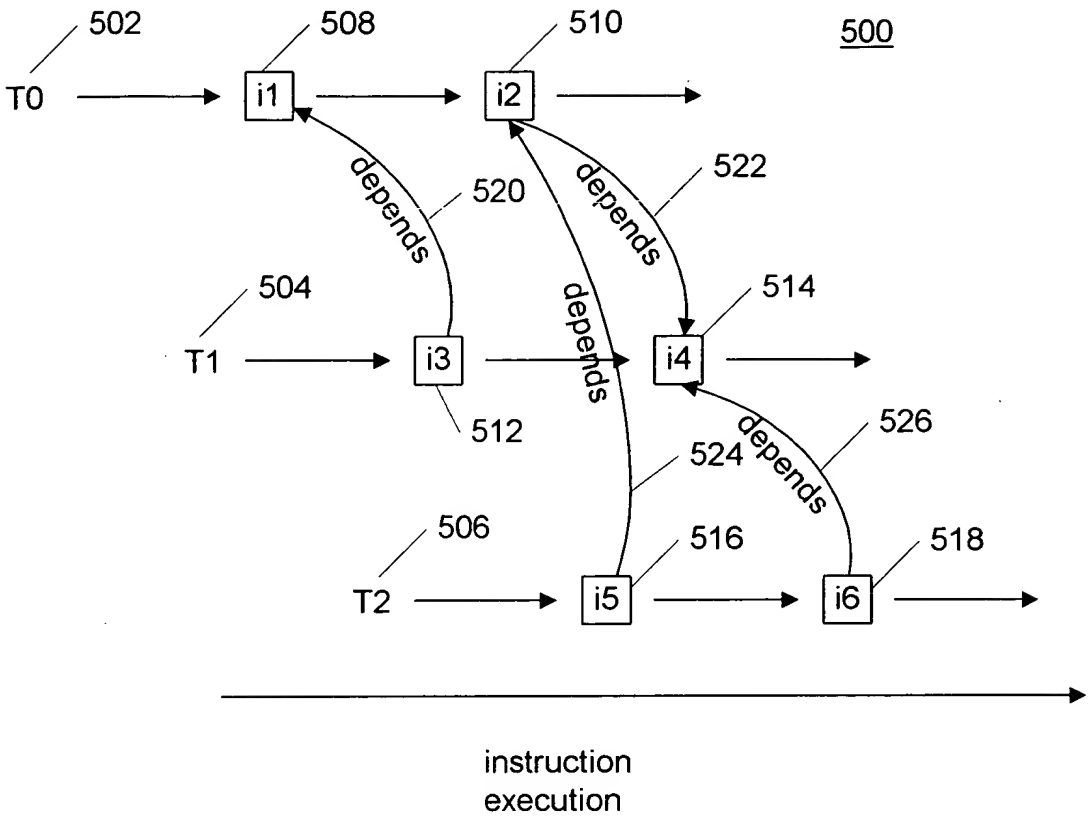
502
508
510
500
T0
i1
i2
depends
520
depends
522
504
514
T1
i3
depends
i4
512
526
524
depends
506
516
518
T2
i5
i6
instruction
execution

FIG. 5

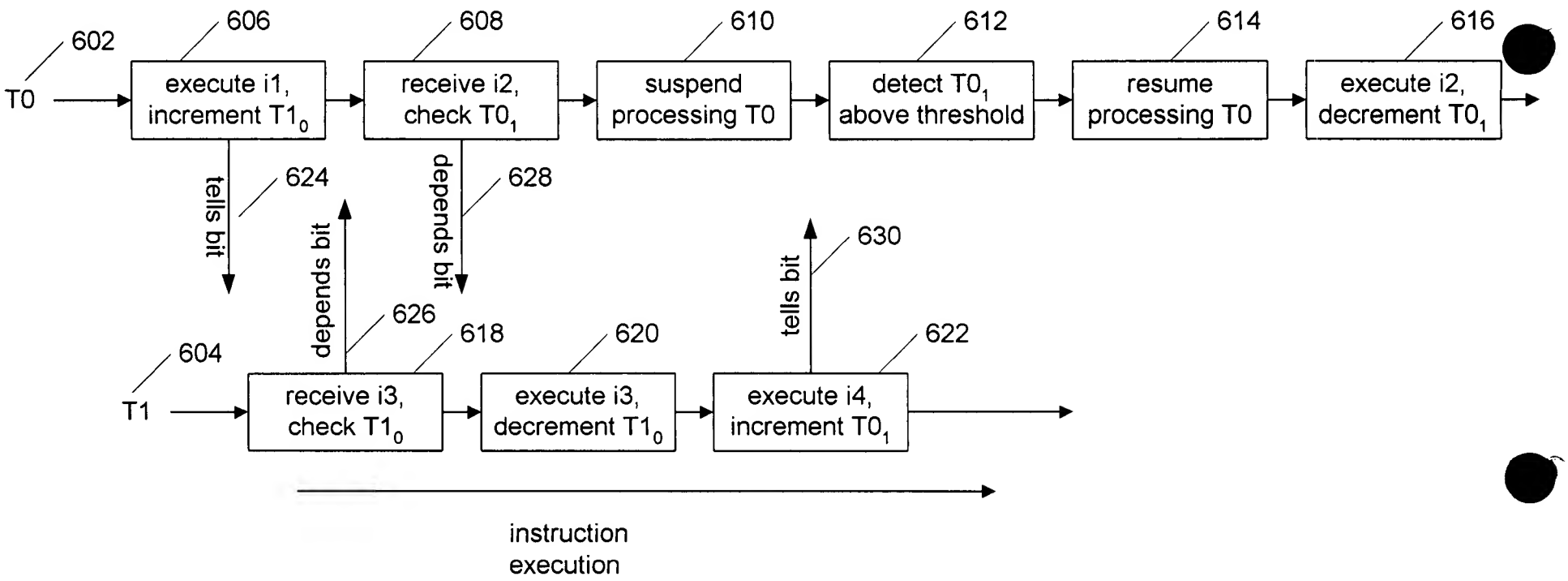
600
602
606
608
610
612
614
616
T0
execute i1, increment T1$_0$
receive i2, check T0$_1$
suspend processing T0
detect T0$_1$ above threshold
resume processing T0
execute i2, decrement T0$_1$
tells bit
624
depends bit
628
depends bit
626
tells bit
630
604
618
620
622
T1
receive i3, check T1$_0$
execute i3, decrement T1$_0$
execute i4, increment T0$_1$
instruction execution

FIG. 6

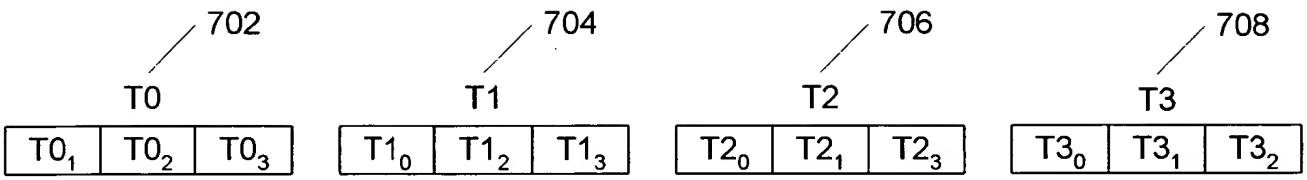

FIG. 7

800

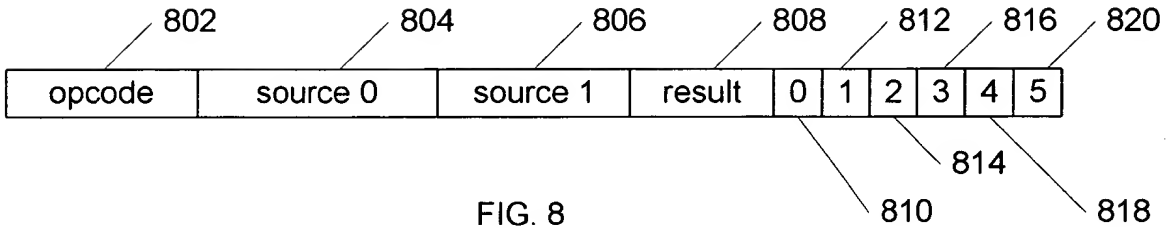

FIG. 8

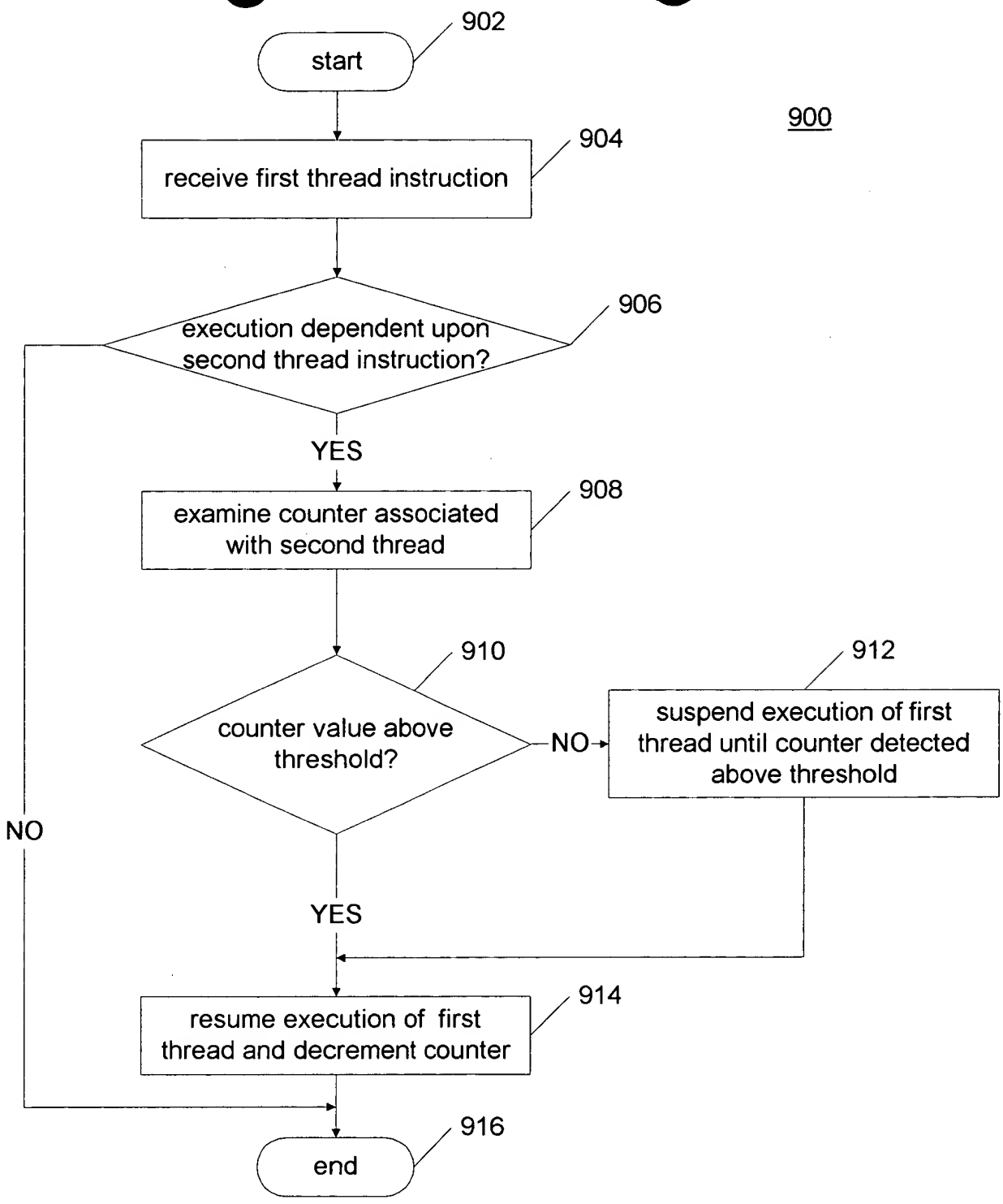
900
902
start
904
receive first thread instruction
906
execution dependent upon second thread instruction?
YES
NO
908
examine counter associated with second thread
910
counter value above threshold?
NO
912
suspend execution of first thread until counter detected above threshold
YES
914
resume execution of first thread and decrement counter
916
end

FIG. 9

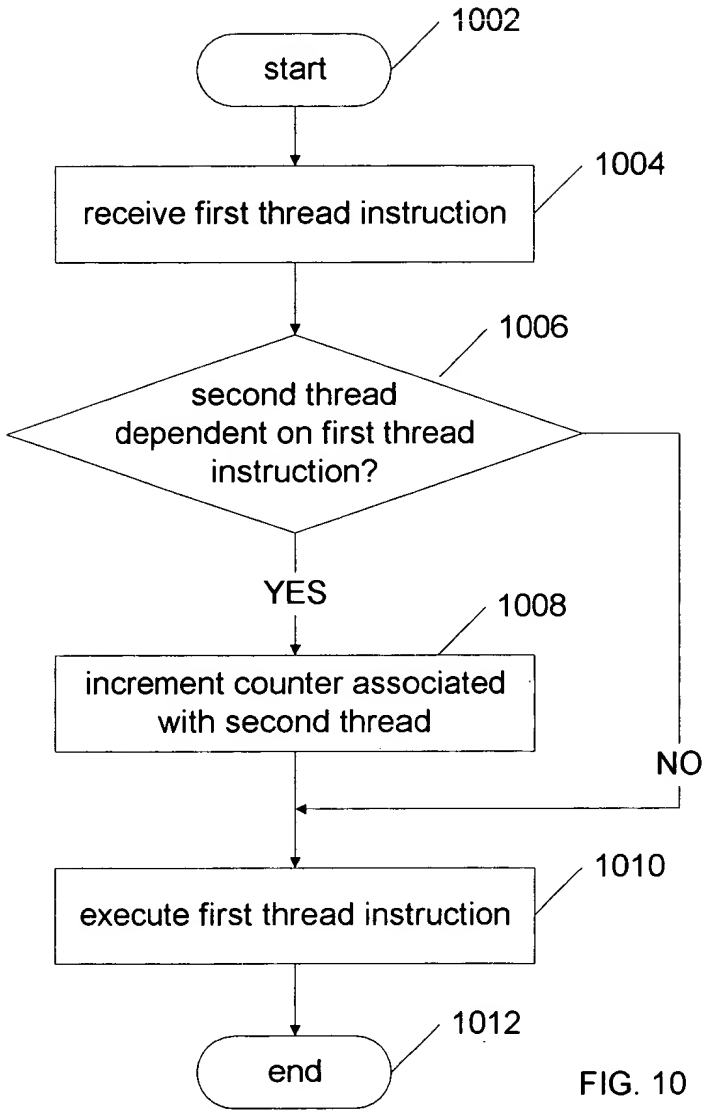
1000
1002
start
1004
receive first thread instruction
1006
second thread dependent on first thread instruction?
YES
NO
1008
increment counter associated with second thread
1010
execute first thread instruction
1012
end

FIG. 10